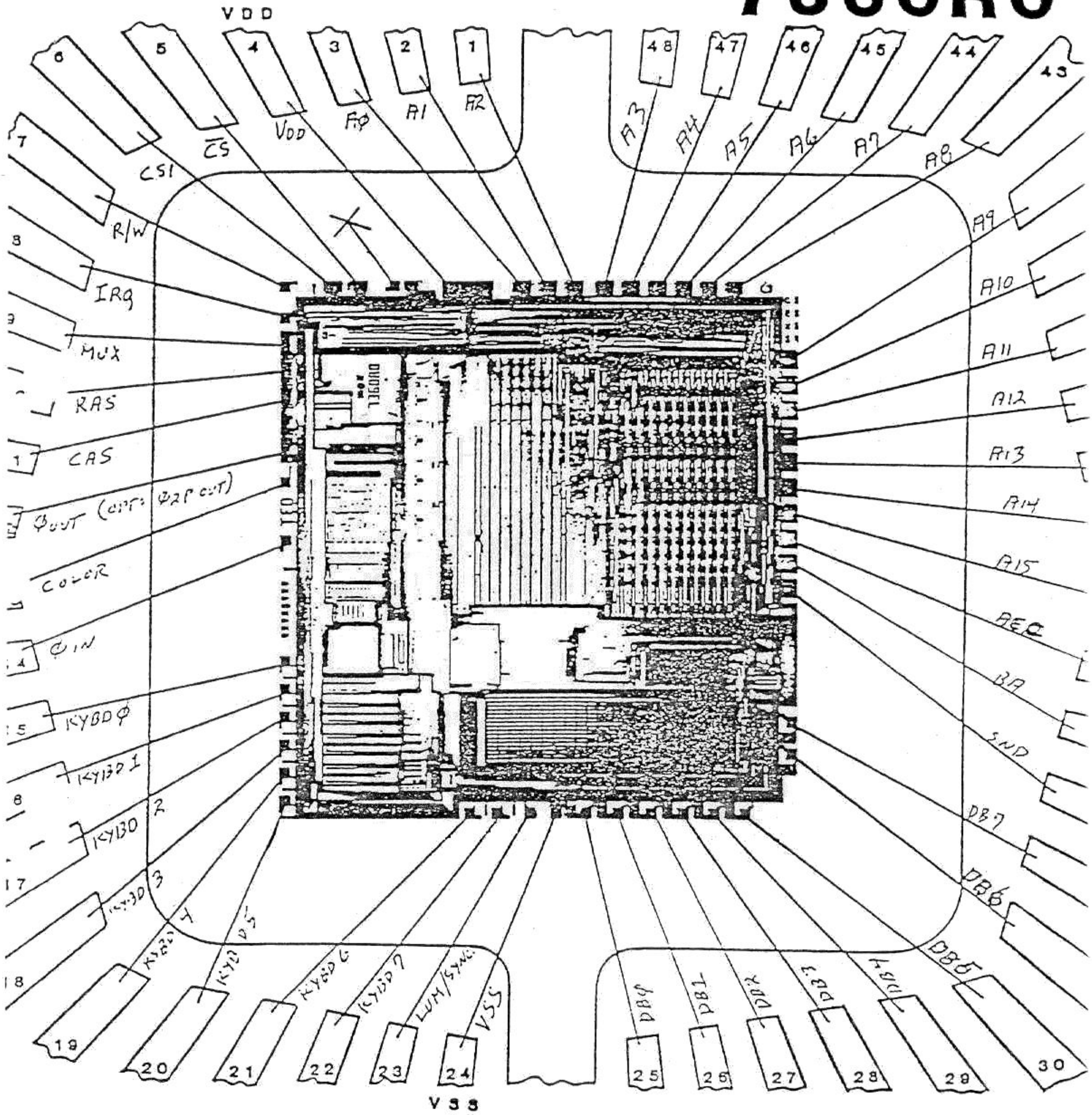
PPROVED: 4/19/83	RELEASED	REV.	DATE	ENGR.	REV.	DATE	ENGR.	REV.	DATE	E

DIE SIZE : X:206 Y:198

7360R0



PACKAGE: 48 LEAD PLASTIC

DIE ATTACH AREA: X:290 Y:280

SCALE: 20X

48 LEAD BONDING DIAGRAM	PAGE OF	SPECIFICATION No.

SCOPE

This specification covers the detailed requirements for a high resolution video display chip utilizing HMOS technologics. This device is intended for use in low end 65Ø2-based personal home computer systems.

The TED chip is a 48 pin device which controls video output, system timing, dynamic RAM control, ROM chip selects, and keyboard control. The TED contains 34 control registers which are accessed through the standard 65Ø2 microprocessor data bus. It will access up to 64K of memory for display information.

CHARACTER MODES

In any of the character modes, the TED chip displays 25 lines of 40 characters per line. Each character on the screen can be set to any of 16 possible colors, with 8 possible luminance levels.

The character pointers in the VIDEO MATRIX determine what character will be displayed in a particular place. Associated with each location of the video matrix is an 8 bit color memory location, called the ATTRIBUTE byte. The attribute byte determines the color, luminance level, and whether that character will flash.

The TED chip fetches character pointers from the area of memory known as the VIDEO MATRIX area, and color information from the ATTRIBUTE area.
The video matrix consists of 1000 consecutive locations in memory, each of which contains an 8 bit character pointer. The location of the video matrix is determined by the VIDEO MATRIX BASE REGISTER in the TED (bits 3-7 of Register #20), which provides the 5 MSB of the video matrix address (A15-A11). The address A10 is always set to a 1. This gives 32 possible locations for the start of the video matrix.

The following chart makes this clear:

BASE ADDRESS	LOCATION	BASE ADDRESS	LOCATION
00000	$0400	10000	$8400
00001	$0C00	10001	$8C00
00010	$1400	10010	$9400
00011	$1C00	10011	$9C00
00100	$2400	10100	$A400
00101	$2C00	10101	$AC00
00110	$3400	10110	$B400
00111	$3C00	10111	$BC00
01000	$4400	11000	$C400
01001	$4C00	11001	$CC00
01010	$5400	11010	$D400
01011	$5C00	11011	$DC00
01100	$6400	11100	$E400
01101	$6C00	11101	$EC00
01110	$7400	11110	$F400
01111	$7C00	11111	$FC00

Each memory location in video matrix is used as a pointer to the actual character dot data which makes up the characters. The eighth (MSB) bit of each of the character pointers (VM7) can be interpreted in two different ways. If the RVS on bit of TED Register 7 is a 0, the MSB of the video matrix (VM7) will determine if the character will be displayed reversed or not. If VM7 is set to 0, the character will be displayed normally. If VM7 is set to a 1, the character at that location will be displayed in reverse. Use of this feature limits the number of different character definitions to 128. If the RVS ON bit is set to a 1, the reverse feature feature is turned off, which allows the use of 256 different character definitions.

VIDEO MATRIX ADDRESS

A15	A14	A13	A12	A11	A1Ø	A9	A8	A7	A6	A5	A4	A3	A2	A1	AØ
VM4	VM3	VM2	MV1	VMØ	1	VC9	VC8	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VCØ

The ATTRIBUTE memory also consists of 1ØØØ consecutive locations, and contains the FLASH bit, the 4 bits of color and the 3 bits of luminance for each character location. The location of the attribute memory is also controlled by the VIDEO MATRIX base register. Like the video matrix, the upper 5 bits of the address of the attributes are the VIDEO BASE REGISTER. However, for attribute memory, A1Ø is always set to a Ø, so is always 1K below the video matrix. For example, if the video matrix is at $ØCØØ, the attribute bytes are at $Ø8ØØ.

ATTRIBUTE MEMORY ADDRESS

A15	A14	A13	A12	A11	A1Ø	A9	A8	A7	A6	A5	A4	A3	A2	A1	AØ
VM4	VM3	VM2	VM1	VMØ	Ø	VC9	VC8	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VCØ

Each character is matrix of 8 by 8 dots, stored in the character ROM as 8 consecutive bytes. The location of this CHARACTER memory is set by CB4 to CBØ of TED Register 19. These bits are used as the 5 most significant bits of the character base address. The next 8 bits of the address of a particular character pattern come from the value of that particular location in the video matrix. (The last 3 bits come from a counter.)

CHARACTER DATA ADDRESS

A15	A14	A13	A12	A11	A1Ø	A9	A8	A7	A6	A5	A4	A3	A2	A1	AØ
CB5	CB4	CB3	CB2	CB1	VM7 CØ	VM6 (with REVERSE bit on)	VM5	VM4	VM3	VM2	VM1	VMØ			

STANDARD CHARACTER MODE

In standard character mode, the character display is an 8 dot horizontal by 8 dot vertical character location formatted in 25 rows of 4Ø characters per row. Each character location in the video matrix has a unique color set by its attribute byte and share a common background color. Eight sequential bytes from character memory are displayed directly on the 98 lines of each character location. A 'Ø' bit causes the color/luminance in background color register Ø to be used; a '1' bit causes the color/luminance of the associated byte of attribute memory to be displayed.

bit of character data	color source	luminance source
Ø	background reg Ø, bits Ø-3	bkgd reg Ø, bits 4-6
1	attribute bits Ø-3	attribute bits 4-6

MULTICOLOR CHARACTER MODE

Multicolor character mode provides additional color flexibility (up to four colors per character location) at a cost reduced horizontal resolution. Multicolor mode is selected by setting the multicolor bit (TED Register 7) to a 1. This causes the data in character memory to be interpreted in a different manner. When in multicolor mode, if bit 3 of the attribute byte is a Ø the character at that location will be displayed as normal (hires) character. If bit 3 of the attribute is a 1, that character will be displayed as a multicolor character. This alllows the two character types to be mixed on a single screen. Only the first 8 colors are available as foreground colors, however. When a character is displayed in multicolor, the character data is defined as eight sequential bytes of character, with 4 dot pairs per byte. The character is displayed as a 4 by 8 dot matrix, with the horizontal dots twice as wide as in standard character mode. The dot pairs are interpreted as follows:

dot pair	color source	luminance source
ØØ	bkgd reg Ø, bits Ø-3	bkgd reg Ø, bit 4-6
Ø1	bkgd reg 1, bits Ø-3	bkgd reg 1, bits 4-6
1Ø	bkgd reg 2, bits Ø-3	bkgd reg 2, bits 4-6
11	attribute bits Ø-2	attribute bits 4-6

Each character location can contain 4 colors, one unique to the character location, the other 3 in common with all other characters on the screen.

EXTENDED COLOR MODE

EXTENDED COLOR MODE allows the individual selection of both background and foreground colors in each character location on the screen. Each character location can select one of the 16 foreground colors and one of 4 available background registers. The character dot data is displayed as in standard color mode (with foreground color/luminance determined by the attribute for a '1' data bit), but the two MSB of the character pointer are used to select the background color/luminance for that screen location. Since the 2 MSB of the character pointer are in use, this means that only the first 64 character definitions in the character memory are available. (The TED chip forces A1Ø and A9 to Ø).

BACKGROUND COLORS

Bits 6 & 7 character pointer	color source	luminance source
ØØ	bkgd reg Ø, bits Ø-3	bkgd reg Ø, bits 4-6
Ø1	bkgd reg 1, bits Ø-3	bkgd reg 1, bits 4-6
1Ø	bkgd reg 2, bits Ø-3	bkgd reg 2, bits 4-6
11	bkgd reg 3, bits Ø-3	bkgd reg 3, bits 4-6

STANDARD (HIRES) BIT MAP MODE

In bit map mode there is a one to one correspondence between each displayed dot and memory bit. Standard bit map mode provides a screen resolution of 320 dots by 200 vertical dots. Each 8 by 8 square (corresponding to the character locations in standard character mode) can have an individually controlled background and foreground color.

The start of the bit map data area comes from the BIT MAP BASE register. The 3 bits of the bit map base are used as the A15-A13 of the address. The bit map data area is 8K, therefore bit map areas must start on 8K boundaries.

BIT MAP BASE	ADDRESS
000	$0000
001	$2000
010	$4000
011	$6000
100	$8000
101	$A000
110	$C000
111	$E000

When in bit map mode, both the video matrix and the attribute memory are used for color data. The address of the bit mapped data is formed by combining the 3 bit BIT MAP BASE register as the MSB of the data address with the 10 bit character position counter and the 3 bit raster counter. This addressing scheme results in each 8 sequential memory locations being formated as an 8 by 8 block on the video display, something like this:

```
byte 0      byte 8      byte 16.................................byte 312
byte 1      byte 9      byte 17.................................byte 313
byte 2      byte 10     byte 18.................................byte 314
byte 3      byte 11     byte 19.................................byte 315
byte 4      byte 12     byte 20.................................byte 316
byte 5      byte 13     byte 21.................................byte 317
byte 6      byte 14     byte 22.................................byte 318
byte 7      byte 15     byte 23.................................byte 319

byte 320    byte 328    byte 336................................byte 632
byte 321    byte 329    byte 337................................byte 633
byte 322    byte 330    byte 338................................byte 634
byte 323    byte 331    byte 339................................byte 635
byte 324    byte 332    byte 340................................byte 636
byte 325    byte 333    byte 341................................byte 637
byte 326    byte 334    byte 342................................byte 638
byte 327    byte 335    byte 343................................byte 639
```

etc.

(or it could be represented like this:)

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
BB2	BB1	BB0	CP9	CP8	CP7	CP6	CP5	CP4	CP3	CP2	CP1	CP0	VS2	VS1	VS0

When in standard bit map mode, the color information is derived from the data stored in the video matrix, while the luminance information comes from the attribute data. This allows for 2 colors to be independently selected in each 8 by 8 area. When the bit to be displayed is a 'Ø', the color of the dot output is set by the lower 4 bits of the video matrix; the luminance is selected by bits 4-6 of attribute memory. When a bit to be displayed is a '1', the color is set by the upper 4 bits of the video matrix; the luminance is set by bits Ø-2 of attribute memory.

dot	color source	luminance source
Ø	video matrix bits Ø-3	attribute bits 4-6
1	video matrix bits 4-6	attribute bits Ø-2

MULTICOLOR BIT MAP MODE

MULTICOLOR bit map mode bears the same relationship to standard bit map mode as multicolor character mode does to standard character mode. Multicolor bit map mode allows greater color selection at the cost of horizontal resolution. Using multicolor mode, up to four different colors can be displayed in each 8 by 8 bit block.

The bit map data area is addressed exactly the same as in standard bit map mode. The dot data and color information is interpreted differently, however.

Multicolor bit map mode is selected by setting both the multicolor bit and the bit map bit to '1'.

As in multicolor character mode, multicolor bit map mode uses the concept of 'dot pairs' to specify one of our pixel colors. Sinc two bits select one dot color, the horizontal resolution is halved (160H by 2ØØV). Each multicolor pixel is twice as wide as hires pixel.

dot pair	color source	luminance source
ØØ	bkgd reg Ø, bits Ø-3	bkgd reg Ø, bits 4-6
Ø1	video matrix bits 4-7	attribute, bits 4-6
1Ø	video matrix bits Ø-3	attribute, bits 4-6
11	bkgd reg 1, bits Ø-3	bkgd reg 1, bits 4-6

Hardware Cursor

The hardware cursor is controlled by a 10 bit cursor compare register (Register 12 and 13). This allows 1024 possible positions. Setting the cursor compare register bits to a value from 0 to 999 results in the cursor appearing in the specified location (the top left corner of the screen is 0, the bottom right corner is 999, etc.). The cursor will blink at the rate of 2Hz, by switching the foreground and background colors in that location. Note: The hardware cursor can only appear during standard character mode.

Flash

The TED chip provides the ability to Flash any or all characters on the screen when using standard character mode, when the TED chip Flash bit is enabled. Flash is selected on a character by character basis, via the MSB of the attribute memory location for that character. When a character is flashing the foreground color of that character will turn off (change to background color) and on again at the rate of 2Hz.

Dynamic Ram Refresh

Dynamic RAM refresh operation is controlled by the TED chip. Five, RAS only refreshes are performed during every raster line, immediately following character fetches. TED guarentees a maximum delay of 3.26msec between the refresh of a single row address in a 256 address refresh scheme. This refresh is totally transparent to the system, since refresh occurs during phase one of the single speed system clock.

System Clock Doubling

For increased processor throughput, the system clock output from TED doubles frequency from 894KHz (NTSC) to 1.788KHz (NTSC), during non-display times. The horizontal position register counts 456 dots, 0 to 455. During counts of 400-344, while in raster lines 0 to 204, the TED device outputs single clock. During this time TED is doing processor handshaking (counts 400-432), character fetches (counts 432-304), and dynamic RAM refresh (counts 304-344). Outside of this horizontal window TED outputs double clock (1.788KHz). During raster lines 205-261 for NTSC (205-311 for PAL), TED outputs double clock at all times except horizontal counts 304-344 which are single clock to allow for dynamic RAM refresh. If the blanking bit (Register #6) is cleared, the active display is cleared, the screen is filled with border color, and double clock is enabled at all times except refresh.

Sound

The TED device has two separate square wave generators. The frequency base for voices 1 and 2 are 10 bit registers (Register #24 and 18 for Voice 1 and Register #15 and 16 for Voice 2. Voice 2 can be selected to be either a square wave generator or a white noise generator. The voice selection and volume control mechanism is Register #17. There are 9 volume levels in TED, ranging from 0 being off to 8 being loud. Programming values of 9-15 in the lower nybble at this register is identical to programming the loudest, volume

8, level. Bits 4-6 of this register each individually select Voice 1, Voice 2, or white noise respectively. Voice 2 and white noise cannot be enabled together, instead Voice 2 selection will override white noise selection. The frequency generated by TED is:

$$\text{FREQUENCY} = \frac{111860.781}{(1024-x)} \quad \text{for NTSC}$$

$$= \frac{110840.45}{(1024-x)} \quad \text{for PAL}$$

A sampling frequency chart follows.

NOTE	BASE REGISTER VALUE (1Ø28-x)	ACTUAL FREQUENCY (HZ)
A	1Ø17	11Ø
B	9Ø6	123.5
C	855	13Ø.8
D	762	146.8
E	679	164.7
F	641	174.5
G	571	195.9
A	5Ø8	22Ø.2
B	453	246.9
C	428	261.4
D	381	293.6
E	339	33Ø
F	32Ø	349.6
G	285	392.5
A	254	44Ø.4
B	226	494.9
C	214	522.7
D	19Ø	588.7
E	17Ø	658
F	16Ø	699
G	143	782.2
A	127	88Ø.7
B	113	989.9
C	1Ø7	1.Ø45K
D	95	1.177K
E	85	1.316K
F	8Ø	1.398K
G	71	1.575K

Internal Operation

All internal timing operations are based on the horizontal dot counter. Particular events occur in response to certain counts of both the horizontal position register and the vertical line register.

HORIZONTAL DECODES			HORIZONTA COUNT
Horizontal Sync		Start	358
		Stop	390
Horizontal Equilization	Pulse 1	Start	152
		Stop	170
	Pulse 2	Start	380
		Stop	398
Horizontal Blanking		Start	344
		Stop	416
Burst		Start	384
		Stop	408
Character Window		Start	432
		Stop	296
External Fetch Window		Start	400
		Stop	288
Refresh Single Clock		Start	288
		Stop	328
Character Window Single Clock		Start	432
		Stop	296
40 Column Screen		Start	451
		Stop	315
38 Column Screen		Start	3
		Stop	307
Video Shift Register		Start	440
		Stop	304
Increment Blink			336
Increment Vertsub Counter			
Increment Refresh		Start	296
		Stop	336
Increment Character Position Reload			424
Increment Character Position		Start	432
		Stop	288
Latch Character Position to Reload			290
End of Screen - Clear Vertical Line, Vertical Sub and Character Reload Registers			384
Increment Vertical Line			376

Many of the events are qualified by a vertical line count.

VERTICAL DECODES				VERTICAL COUNT
End of Screen PAL				311
End of Screen NTSC				261
Vertical Sync	PAL	Start		254
		Stop		257
	NTSC	Start		229
		Stop		232
Vertical Equalize	PAL	Start		251
		Stop		260
	NTSC	Start		226
		Stop		235
Vertical Blanking	PAl	Start		251
		Stop		269
	NTSC	Start		226
		Stop		244
Attribute Fetch	Start			0
	Stop			203
Frame Window	Stop			204
Vertical Screen Window	25 Row	Start		4
		Stop		204
	24 Row	Start		8
		Stop		200

TED REGISTER DESCRIPTION

Internal Timers, Register Ø through 5

Ted contains three 16 bit decrementing interval timers, each partitioned into 2, 8 bit registers. To initiate a new count value, loading the low Byte inhibits counting until the high Byte is loaded. The timers decrement at a 894 KHZ rate for NTSC television systems, 884 KHZ for PAL systems. Each counter generates an interrupt upon decrementing to Ø. The sequence for writing to the timers should be:

Disable all interrupts
Write low Byte
Write high Byte
Enable desired interrupts

Care should be taken that long time intervals, more than 125u seconds, do not occur between writing the low and then the high Bytes.

Timer 1 is a sequence interval timer. Registers Ø and 1 when written to initiate the reload value of the timer. When timer 1 is decremented to Ø, the next count occurs from the reload value. Reading Registers Ø and 1 gives the current count valve.

Timers 2 & 3 are free running counters. Upon decrementing to Ø the timers roll over to FF and continue counting. Writing to timer 2 and 3 registers loads directly into the active count. Reading these registers yields the current count.

Register 6

Bits Ø-2 of this register determine the vertical scroll position. For a normal 25 row picture with no scroll these bits should be a '3'. Bit 3 is the 24/25 row select. A 'Ø' in this bit corresponds to 24 rows and a '1' yields 25 rows. For vertical scroll to occur, bit 3 should be cleared and bits Ø-2 all set. Decrementing bits Ø-2 moves character position up scrolling off the uppermost charcter row. Bit 4 is the blanking bit. Setting this bit to a '1' gives a normal picture. Setting it to a 'Ø' blanks the screen and disables all fetches from occuring, allowing for the system clock to run at twice the frequency (1.788MHZ NTSC, 1.768MHZ for PAL) except for 5 refresh cycles per raster line. Bits 5 and 6 are display mode Bits. Setting Bit 5 to a '1' enables Bit mapped mode, while setting bit 6 enables extended color mode. Bit 7 is a bit used for I.C. testing and must remain a 'Ø'.

Register 7

Bits Ø-2 determine the horizontal scroll position. A 'Ø' in these bits allows for no scroll. To institute scroll bit 3 of this register, the 38/4Ø column bit, should be set to 'Ø'. This displays 38 columns and scroll can occur cleanly. Incrementing the 3 LSB of this register pans the character positions to the right.

Bit 4 is multicolor mode bit. Setting this bit to '1' enables multicolor. The freeze bit is bit 5. Setting freeze high stops TED from incrementing the horizontal position, the timers and the vertical position. The system is forced into single clock (894KHZ) and system refresh of dynamic rams. Bit 6 is PAL/. Setting this bit high forces NTSC mode, low corresponds to the PAL mode. Bit 7 is the reverse video off bit. Under normal conditions, bit 7=Ø, there are 128 character locations. The reverse video character is implimented by setting the MSB of the video matrix pointer to a '1'. This enables the TED chip to invert the character data and thus reverse video. If an alternate character set of 256 locations is desired, this bit can be set high turning the reverse video feature off and allowing the MSB of the video matrix to define the additional character locations.

Register 8

This register is the keyboard latch. Writing to Register 8 scans the keyboard lines and latches the appropriate data. Reading the register, reads the latched data.

Register 9

The interrupt register indicates any TED interrupt source. Possible interrupt sources are:

Bit 1	raster interrupt	-compares raster register to active count
Bit 3	timer 1 interrupt	-timer 1 has decremented to 'Ø'
Bit 4	timer 2 interrupt	- " 2 " " " " "
Bit 6	" 3 " "	- " 3 " " " " "

Bit 2 indicates a light pen interrupt. The TED computer does not have light pen. This bit is for future expansion. Bit 7 is the interrupt bit. It is the inversion of the interrupt pin. Writing a '1' to the interrupt register clears the individual interrupt bit.

Register 1Ø

Register 1Ø is the interrupt mask register. The individual mask bit corresponds to each of the possible interrupt sources. Setting the bit high enables interrupts to occur. The LSB of this register is the MSB of the raster register. (see Register 11 description)

Register 11

In an NTSC television system, 262 raster lines are produced (Ø to 261), 312 for PAL (Ø-311). To detect all possible raster lines a 9 bit register is needed. Register 11 contains the low order 8 bits of this raster register. Register 1Ø contains the MSB. The raster register is an interrupt source. The raster register value is compared to the current vertical line count. An interrupt is generated 8 cycles before the character window. For a 25 row display the visible raster lines are from 4 to 2Ø3.

Register 12

Register 12 contains the 2 MSB of the cursor position register. Bits Ø and 1 correspond to cursor bits 8 and 9.

Register 14

Register 14 contains the low byte of Voice 1 frequency base. All TED sound generators produce square waves.

Register 15

The low order eight bits of the frequency base for the second voice source are contained in this register. This voice is selectable for either white noise or another square wave generator. This selection is available in Register 17.

Register 16

This register contains the 2 MSB of Voice 2.

Register 17

Register 17 has 4 bits of volume control ranging from Ø = OFF to '8' being loud. Also 3 voice selects are available. Voice 1 select, Voice 2 square wave select and Voice 2 white noise select. The MSB of this register is a bit used for testing. The sound reload bit will clear the sound toggle flops and initiate the reload value of each voice to initialize the active sound count during the appropriate voice incrementing time. This bit will also initiate the white noise random number generator to '1's.

Register 18

This register contains the three bit bit map mode address base, the ROM/RAM bank bit, and the 2 bit MSB of voice 1 frequency base. The bit map base determines where in the memory map the bit map dot data can reside. Bits 3 through 5 correspond to BMB0 to BMB2. During TED dot fetches in the bit map mode, BMB2 will become A15, BMB1 - A14, and BMB0-A13. The ROM/RAM bank bit, bit 2, will force TED dot and character fetches from either ROM or RAM. A '1' in this bit will force ROM execution a '0' will force RAM.

Register 19

This register contains the character base, force single clock bit, and the status bit. The force single clock bit, when set high, inhibits the PH out of TED from doubling frequency during horizontal blanking. The status bit is a read only bit indicating the state of the 2 phantom Registers 62 and 63. If this bit is high it indicates that TED is operating for the ROM bank memory. This bit does not indicate where TED will fetch character or dot information is coming from.

Register 20

The 5 bit video matrix base, bits 3 through 7, comprise Register 20. The video matrix base determine the memory mapping of the video matrix pointers and the attribute data as shown:

A15	A14	A13	$\overline{\text{A12}}$	A11
VM4	VM3	VM2	VM1	VM0

The attribute and video matrix fetches occur on the raster line preceeding the charactor row (attribute) and the first raster line of the character row. During these fetches TED will DMA the processor and take complete control of the system bus for both halves of the clock cycle, for 40 consecutive clock cycles.

Register 21

This register contains a three bit luminance code and a four bit color code-for background Register 0. This allows for eight separate luminance level for each 16 colors.

Register 22

Register 22 contains the same data as Register 21 for background Register 1.

Register 23

Background Register 2 data is stored here.

Register 24

Register 24 is comprised of luminance and color data for background Register 3.

Register 25

Luminance and color information for the exterior register (border) is stored in Register 25.

Register 26

The two MSB of the character position reload register are bits Ø and 1 of this register. The character position reload increments by forty for each character row completed. For example, during the first character row this register will contain 'Ø'. Upon completion of the eighth raster line of the row the character position bit map reload register will be updated to 4Ø.

Register 27

The low byte of the character position reload register is located here. (See Register 26).

Register 28

This register contains only 1 bit, the MSB of the vertical line register. The vertical line register contains the current raster line being displayed. For NTSC systems this register will count from Ø to 261, for PAL, Ø to 311.

Register 29

The low byte of the vertical line register is contained in Register 29.

Register 3Ø

Register 3Ø is the horizontal position register. Register 3Ø contains the upper 8 bits of this nine bit register. The LSB increments at a rate too fast to be of any use in programming. Since the horizontal position register actually increments from Ø to 455, Register 3Ø will contain values of Ø to 228. Negative true data is to be written to this register while positive true data is read.

Register 31

This register contains the 4 bit blink rate register and the 3 bit vertical subaddress register. The blink rate register contains the current count of the blink rate timer. This register is incremented once per screen. On overflow a 2HZ signal is generated initalizing the cursor reverse video and any flashing characters. The vertical subaddress counts the eight raster line per character row.

Registers 62 and 63

These registers do not physically exist on the TED chip. A write to these locations controls the TED system memory map. Any write to Register 62 results in ROM being selected in memory locations $8ØØØ(HEX) to $FFFF(HEX) excluding $FDØØ(HEX) to $F3FF(HEX) for I/O space and TED space. The TED chip will generate the necessary chip selects and inhibit CAS until a write to Register 63 occurs. Upon this occurrence, the same locations $8ØØØ(HEX) to $FFFF(HEX) excluding $FDØØ(HEX) to $F3FF(HEX) are banked to RAM. CAS occurs when appropriate and chip selects are suspended.

All TED registers, unless otherwise noted, are read/write. It should be noted that care should be taken when writing to Register 26 through 31. These are internally controlled registers. Writing to them can result in a flicker on the screen.

PINOUT

PIN #	DESIGNATION	SIGNAL DIRECTION	SIGNAL POLARITY	DESCRITPION
1	A2	input/output	+true	address bit 2
2	A1	" "	"	" " 1
3	AØ	" "	"	" " Ø
4	VDD	input	5V	power supply
5	CSØ	output	-true	low ROM chip select
6	CS1	output	"	high ROM chip select
7	R/W	input/output	+true	read/write
8	IRQ	output	-true	interrupt
9	MUX	output	"	address multiplex switch
1Ø	RAS	"	"	RAM row address strobe
11	CAS	"	"	RAM column address strobe
12	Øout	"	"	894.9KHZ CPU clock (NTSC) 886.7KHZ CPU clock (PAL)
13	COLOR	"	+true	chrominance
14	Øin	input	"	14.31818MHZ single phase +/- 1Ø% (NTSC) 17.734475MHZ single phase +/- 1Ø% (PAL)
15	KØ	input/int pullup	"	keyboard latch Ø
16	K1	" " "	"	" " 1
17	K2	" " "	"	" " 2
18	K3	" " "	"	" " 3
19	K4	" " "	"	" " 4
2Ø	K5	" " "	"	" " 5
21	K6	" " "	"	" " 6
22	K7	" " "	"	" " 7
23	LUM	output	"	composite sync and luminance
24	VSS	input	OV	power supply
25	DBØ	input/output	+true	data bit Ø
26	DB1	" "	"	" " 1
27	DB2	" "	"	" " 2
28	DB3	" "	"	" " 3
29	DB4	" "	"	" " 4
3Ø	DB5	" "	"	" " 5
31	DB6	" "	"	" " 6
32	DB7	" "	"	" " 7
33	SND	output	+true	sound
34	BA	output	+true	bus available
35	AEC	"	"	tri-state control
36	A15	input/output	"	address bit 15
37	A14	" "	"	" " 14
38	A13	" "	"	" " 13
39	A12	" "	"	" " 15

PIN #	DESIGNATION	SIGNAL DIRECTION	SIGNAL POLARITY	DESCRIPTION
4Ø	A11	input/output	+true	address bit 11
41	A1Ø	" "	"	" " 1Ø
42	A9	" "	"	" " 9
43	A8	" "	"	" " 8
44	A7	" "	"	" " 7
45	A6	" "	"	" " 6
46	A5	" "	"	" " 5
47	A4	" "	"	" " 4
48	A3	" "	"	" " 3

PIN FUNCTIONS

ADDRESS BUS   pins 1 thru 3 and 36 thru 48

The 16 bit address bus is bidirectional. As an input, the microprocessor can access any of the 34 TED control registers. In the output mode TED uses the addresses to fetch Video Matrix Pointers, Attribute Pointers or character cell information. For microprocessor interface TED resides in locations FF00-FF3F in memory.

DATA BUS   pins 25 thru 36

The 8 bit data bus is also bidirectional. The data bus activity can be separated into 2 categories: microprocessor interface and video data interface during the above mentioned fetches.

KEYBOARD LATCH   pins 15 thru 22

The 8 bit keyboard latch is used as the keyboard interface. Upon an instruction by the microprocessor to write to the keyboard latch, the information on the keyboard pins is latched by TED and stored until it is retrieved by the microprocessor on a read keyboard instruction. The keyboard pins also provide the active pull up on the keyboard matrix lines. These pull ups source a minimum 600μ amps and maximum 900m Amps current. The trip point of the keyboard latch is 2.0 Volts.

Two of the keyboard pins also provide testing functions. When these pins are externally driven to 10 volts, they provide specific testing features. K0 generates a system freeze function, stoping the horizontal counter, thus freezing the position, and sets all horizontal flip-flops to force TED into the dynamic RAM refresh period and single clock. All flip-flops are then released to allow their manipulation by the horizontal register. K1 forces the internal clock division into the NTSC mode.

CHIP SELECTS   pins 5 and 6

Ted generates ROM chip selects based on address decoding. CS0 is active during the memory block of 8000-BFFF (HEX). CS1 corresponds to C000-FFFF (HEX) in memory. The ROM area of memory can be banked out to overlay RAM, see the description of Registors 3E and 3F (HEX).

DYNAMIC RAM CONTROL   pins 9 thru 11

TED generates RAS and CAS for dynamic RAM access. The signal MUX is also generated to externally multiplex the RAM row and column addresses.

READ/WRITE   pin 7

R/W is an input to TED to distinguish the type of operation to be performed. TED will actively pull up the system read line during all TED fetches. The read signal is qualified with MUX. The pin is an open source output.

INTERRUPT pin 8

The interrupt pin is an open drain output. TED contains four interrupt sources: 3 internal timers and the raster comparator.

ØOUT pin 12

For increased processor throughput, TED doubles the frequency of th system clock during horiztonal and vertical blanking. The actual single clock boundries are:

1) raster lines Ø-2Ø4 and horizontal positions 4ØØ-344
2) horizontal positions 3Ø4-344

ØIN pin 14

For use in NTSC television systems, TED requires a 14.31818MHZ single phase clock input. For PAL systems, the input clock must be 17.734475MHZ single phase.

COMPOSITE COLOR pin 13

The color output contains all chrominance information, including the color reference burst signal and the color of all display data. The color output is open source and should be terminated with 1K ohms to ground.

COMPOSIT SYNC AND LUMINANCE pin-23

The luminance output contains all video synchronization as well as luminance information of the video display. This pin is open drain, requiring an external pullup.

SOUND pin 33

This pin provides the output of the 2 tone generators. The output must be integrated through an RC network and then buffered to drive an external speaker.

US AVAILABLE pin 34

Bus Available indicates the state of TED with respect to video memory fetches. BA will go low during phase 1, 3 single clock cycles before TED performs any memory access and will remain low for the entire fetch.

ADDRESS ENABLE CONTROL pin 35

During double clock mode, AEC is always high allowing the 651Ø complete control of the system buses. For single clock time periods, when BA has not gone low, AEC will toggle with Ø2out. This allows TED PHi1, time to complete its memory accesses of video dot information while the 651Ø performs during PHi2. When TED needs both halves of the cycle to perform it customary PHi1 dot fetches and PHi2 attribute and pointer fetches, BA will go low. On the fourth PHilout, AEC will remain low until the end of the PHi2 video fetch.

7360R7 TIMING SPECIFICATIONS ----------NTSC ONLY----------

	Single clock lo		Single clock hi		Double clock lo		Double clock hi	
	min	max	min	max	min	max	min	max
Tcyc in	69.81	69.88						
PW in lo	25	45						
PW in hi	25	45						
Tcyc	1117	1118	1117	1118	558	559	558	559
Clock PW	535	585	535	585	275	295	260	285
Tclkras lh	60	110	60	110	60	110		
Tclkrash l	220	260	220	260	220	260		
Tclkmux lh	60	110	60	110	60	110		
Tclkmuxh l	260	290	260	290	260	290		
Tclkcas lh	60	110	60	110	60	110		
Tclkcasrd	300	365	300	365	300	365		
Tclkcaswr			420	470	420	470		
Traslmux l	20		20		20			
Tmuxlcas l	35		35		35			
Traslcas l	75		75		75			
Tcaswrash	160		160		160			
Tclkcas l		305		305		305		305
Tclkcsh	40	110	40	110				110
Tc.lkaec	10	40	10	40				
PWras lo	360	440						
PWras hi	120	200						
PWcas lo	170	360						
PWcas hi	200	390						
Taddoutac		150		150				
Taddoutr l		40		40				
Tdoutstp			160				160	
Tdouth ld			40	120			40	120
Tdinstp		90		90				90
Tdinh ld		10		10				410
Taddinstp				400				400
Taddinh ld				0				0

COMMODORE		TITLE
DRAWING NO.	REV	SCALE
		SHEET OF